IN THE CLAIMS:

Please amend Claims 11, 12, and 18, as indicated below. The following is a complete listing of claims and replaces all prior versions and listings of claims in the present application:

Claims 1 - 10 (cancelled).

Claim 11 (currently amended): A method of manufacturing a semiconductor apparatus provided with both a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor, said method comprising:

forming a first conductive type impurity region in respective channel positions of said buried channel type MOS transistor and said surface channel type MOS transistor in a same step, such that a lowest potential region within said buried channel type MOS transistor, in comparison to potentials of other regions of an under portion of a gate of said buried channel type MOS transistor, is arranged in an area that is at a predetermined depth from a surface of ~~an image pickup device of~~ said semiconductor apparatus.

Claim 12 (currently amended): A method of manufacturing a solid state image pickup device having a photoelectric conversion portion and a pixel including a plurality of transistors formed in correspondence to said photoelectric conversion portion, in a substrate, wherein said plurality of transistors includes a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor, said method comprising:

forming a first conductive type impurity region in respective channel positions of said buried channel type MOS transistor and said surface channel type MOS transistor, such that a lowest potential region within said buried channel type first conductive type MOS transistor, in comparison to potentials of other regions of an under portion of a gate of said buried channel type first conductive type MOS transistor, is arranged in an area that is at a predetermined depth from a surface of the image pickup device.

Claim 13 (previously presented): A method of manufacturing a solid state image pickup device as claimed in claim 12, said method further comprising forming a second conductive type impurity region in a channel region of said surface channel type MOS transistor, to control a threshold voltage used as a turn-off voltage.

Claim 14 (previously presented): A method of manufacturing a solid state image pickup device as claimed in claim 13, wherein a dose amount of dopants used to dope said first conductive type channel region is smaller than a dose amount used to dope said second conductive type channel region.

Claim 15 (previously presented): A method of manufacturing a solid state image pickup device as claimed in any one of claims 12 to 14, wherein said first conductive type is an n-type.

Claim 16 (previously presented): A method of manufacturing a solid state image pickup device as claimed in claim 15, wherein arsenic is used as a dopant to dope said first conductive type channel region.

Claim 17 (previously presented): A method of manufacturing a solid state image pickup device as claimed in claim 12, wherein a gate electrode of said buried channel type first conductive type MOS transistor is formed of polysilicon doped with an impurity of said second conductive type, and wherein a gate electrode of said surface channel type first conductive type MOS transistor is formed of polysilicon doped with an impurity of said first conductive type.

Claim 18 (currently amended): A method of manufacturing a solid state image pickup device having a photoelectric conversion portion and a pixel including a plurality of transistors formed in correspondence to said photoelectric conversion portion, in a substrate, said method comprising:

forming said plurality of transistors to include a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor;

forming a first conductive type impurity region in respective channel portions of said buried channel type MOS transistor and said surface channel type MOS transistor, such that a lowest potential region within said buried channel type MOS transistor, in comparison to potentials of other regions of an under portion of a gate of said buried channel type MOS transistor, is arranged in an area that is at a predetermined depth from a surface of said image pickup device,

forming a second conductive type impurity region in a channel region of said surface channel type MOS transistor, to control a threshold voltage used for a turn-off voltage,

wherein a gate electrode of said buried channel type first conductive type MOS transistor is formed of polysilicon doped with an impurity of said second conductive type, and

wherein a gate electrode of said surface channel type first conductive type MOS transistor is formed of polysilicon doped with an impurity of said first conductive type.